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Appeal Brief - Patents
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RE: Application No. 09/640,260
Filed: 08/16/2000
Art Unit: 2662
Examiner: Gregory B. Sefcheck
Inv.: Joseph B. Tompkins
Docket No. 00CXT0490N-2
FAX: 571-273-8300

MESSAGE Attached are the following:

1. Transmittal (1 page);
2. Credit Card Payment Form (1 page);
2. Notice of Appeal (1 page);
2. Brief on Appeal (13 pages).

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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

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Filing Date	08/16/2000
First Named Inventor	Joseph B. Tompkins
Art Unit	2662
Examiner Name	Gregory B. Sefcheck
Attorney Docket Number	00CXT0490N-3

ENCLOSURES *(check all that apply)*

- ☐ Fee Transmittal Form
  - ☐ Fee Attached
- ☐ Amendment / Reply
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Reply to Missing Parts/ Incomplete Application
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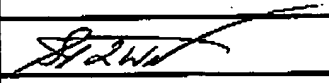
Signature			
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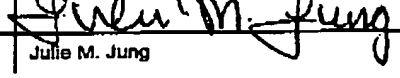
Signature			
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PATENT APPLICATION

ATTORNEY DOCKET NO. 00CXT0490N-2

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): **Joseph B. Tompkins**

Serial No.: **09/640,260** **Examiner: Gregory B. Sefcheck**

Filing Date: **08/16/2000** **Group Art Unit: 2662**

Title: **Integrated Circuit that Processes Communication Packets with a Buffer Management Engine Having a Pointer Cache**

MAILSTOP: Appeal Brief-Patents
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BRIEF ON APPEAL

INTRODUCTION

Pursuant to the provisions of 37 CFR § 1.191 *et seq.*, applicants hereby appeal to the Board of Patent Appeals and Interferences (the "Board") from the examiner's final rejection dated 6/15/2005. A notice of appeal was sent on the same day as this appeal brief. This brief on appeal is accompanied by the requisite fee (37 CFR 41.20(b)(2)), which payment is by credit card. Form PTO-2038 is attached.

REAL PARTY IN INTEREST

08/12/2005 MBINAS 00000028 09640260
02 FC:1402 500.00 OP

The entire interest in the present application has been assigned to Conexant Systems, Inc. as recorded at Reel 011247, Frame 0905.

RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

STATUS OF CLAIMS

Claims 1 – 4, 6 – 21, 23 – 28 and 30 – 34 are pending.

Claims 1 – 4, 6 – 21, 23 – 28 and 30 – 34 have been finally rejected.

Claims 1 – 4, 6 – 21, 23 – 28 and 30 – 34 are on appeal.

STATUS OF AMENDMENTS

There are no pending amendments.

SUMMARY OF INVENTION

The invention is in the field of integrated circuits that process communication packets. The integrated circuit has a buffer management engine that relieves the core processor of significant external buffer management. The buffer management engine also reduces the bandwidth between the integrated circuit and external memory that is required for buffer management. Advantageously, the buffer management engine allows the use of relatively small packet-sized external buffers if desired.

The integrated circuit processes communication packets and comprises a pointer cache and control logic. The pointer cache store pointers that correspond to external buffers that are external to the integrated circuit and configured to store the communication packets. The control logic allocates the external buffers as the corresponding pointers are read from the pointer cache and de-allocates the external buffers as the corresponding pointers are written back to the pointer cache (page 4 line 15 – page 5 line 5).

The control logic tracks the number of the pointers to the de-allocated external buffers. The control logic may transfer additional pointers to the pointer cache if the number of the

pointers to the de-allocated buffers reaches a minimum threshold. The control logic may transfer an exhaustion signal if the number of the pointers to the de-allocated buffers reaches a minimum threshold (page 5 lines 5 – lines 12). To store a packet in an external memory, the core processor must first allocate a external buffer in the memory (page 4, lines 3 – 5).

ISSUES

1. Whether claims 1 – 4, 7 – 9, 12, 13, 18 – 21, 23 – 26 and 30 are unpatentable under 35 U.S.C. § 103(a) over Yu et. al. (US 6,504,846) in view of Koufopaviou (US 5493652).

GROUPING OF CLAIMS

For the purpose of this appeal claims 1 – 4, 6 – 21, 23 – 28 and 30 – 34 stand or fall together.

ARGUMENT

OUTLINE

I. Summary of the brief on appeal.
II. Summary of the requirements for *prima facie* obviousness.
III. Claims 1 – 4, 6 – 21, 23 – 28 and 30 – 34 rejection

I. Summary of the brief on appeal

A. The 35 U.S.C. § 103(a) rejection of claims 1 – 4, 7 – 9, 12, 13, 18 – 21, 23 – 26 and 30 is improper because a *prima facie* case for obviousness has not been established, for the following reasons: (1) the cited art does not teach or suggest every element of the claim, (2) the examiner incorrectly characterizes the cited art.

II. Summary of the requirements for *prima facie* obviousness.

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

MPEP 2143.03

The prior art reference (or references when combined) must teach or suggest all the claim limitations. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974).

If an independent claim is nonobvious under 35 U.S.C. 103, then any claim dependent therefrom is nonobvious. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988).

MPEP 2142.

"To establish a prima facie case of obviousness, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings."

"To establish a *prima facie* case of obviousness, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings." MPEP 2142. "The teaching or suggestion to make the claimed combination... must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck*, 947 F.2ed 488, 20 USPQ2ed 1438 (Fed. Cir. 1991). "The level of skill in the art cannot be relied upon to provide the suggestion to combine references." *Al-Site corp. v. VSI Int'l Inc.*, 174 F.3d 1308, 50 USPQ2d 1161 (Fed. Cir. 1999). "The mere fact that references can be combined or

modified does not render the resultant combination obvious unless the prior art also suggest the desirability of the combination" In re Mills, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990).

III. Claims 1 – 4, 6 – 21, 23 – 28 and 30 – 34 rejection.

Claim 1 has been finally rejected as being unpatentable under 35 U.S.C. § 103(a) over Yu et. al. (US 6,504,846) in view of Koufopaviou (US 5493652). Claim 1 requires:

1. An integrated circuit that processes communication packets, the integrated circuit comprising:

a core processor configured to create a plurality of external buffers that are external to the integrated circuit and configured to store the communication packets where each external buffers is associated with a pointer that corresponds to the external buffer;

a pointer cache configured to store the pointers that correspond to the external buffers;

control logic configured to allocate the external buffers as the corresponding pointers are read from the pointer cache and de-allocate the external buffers as the corresponding pointers are written back to the pointer cache wherein the control logic is configured to transfer an exhaustion signal if a number of the pointers to the de-allocated buffers reaches a minimum threshold; and

the core processor configured to create additional external buffers and their corresponding pointers in response to the exhaustion signal.

Claim 1 has the limitation that "the control logic is configured to transfer an exhaustion signal if a number of the pointers to the de-allocated buffers reaches a minimum threshold". The examiner states that Yu does not disclose transferring an exhaustion signal if the number of the pointers to the de-allocated buffers reaches a minimum threshold. The examiner cites column 3 lines 15 – 20, and column 4 lines 20 – 46 of Koufopaviou as teaching transferring of an exhaustion signal when the number of pointers to the de-allocated buffers reaches a minimum.

The examiner has mischaracterized the cited art. Koufopaviou does not keep track of the number of pointers in the pointer memory. Because Koufopaviou does not keep track of the number of pointers in the pointer buffer, Koufopaviou can not compare the number of pointers to a threshold. Therefore Koufopaviou can not transfer an exhaustion signal when the number of pointers in a buffer falls below a threshold. The cited art talks about a buffer that contains pointers, but the number of pointers in the buffer is not compared to a threshold as required by claim 1. Because Yu and Koufopaviou do not transmits an exhaustion signal if a number of the pointers to the de-allocated buffers reaches a minimum threshold, as required by claim 1, the examiner has not established the requirements for a *prima facie* case of obviousness. Therefore Claim 1 is allowable as written.

Furthermore, in Koufopaviou, even when the number of pointers in the pointer buffer reach zero nothing happens. In fact the main idea in Koufopaviou is to reduce the number of pointers in the pointer buffer to zero, indicating that there are no empty buffers mixed in with the full buffers (i.e. all the empty buffers are in the contiguous empty buffer section). The current invention is completely different in that the object is to maintain at least a minimum number of pointers in the buffer. Claim 1also requires that "the core processor [is] configured to create additional external buffers and their corresponding pointers in response to the exhaustion signal". Koufopaviou does not create additional buffers in response to an exhaustion signal. First Koufopaviou does not generate an exhaustion signal as discussed above. Second Koufopaviou uses a circular buffer with a fixed number of spaces (see figure 1). Because Koufopaviou uses a circular buffer with a fixed number of spaces, Koufopaviou can not create additional buffer even if it received an exhaustion signal. Because Yu and Koufopaviou do not contain a core processor that creates additional buffers in response to the exhaustion signal, as required by claim 1, the examiner has not established the requirements for a *prima facie* case of obviousness. Therefore

Claim 1 is allowable as written.

The prior art reference (or references when combined) must teach or suggest all the claim limitations. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). Here, there are a number of elements required in claim 1 (discussed above) that are not taught by Koufopaviou et al. in combination with Yu et. al. Therefore the examiner has not established a *prima facie* case of obviousness and claim 1 is allowable as written.

Claims 2 – 4 and 6 – 17 are dependent on allowable claim 1 and are therefore allowable.

Claim 18 has been finally rejected as being unpatentable under 35 U.S.C. § 103(a) over Yu et. al. (US 6,504,846) in view of Koufopaviou (US 5493652). Claim 18 requires "transferring an exhaustion signal if a number of the pointers to the de-allocated buffers reaches a minimum threshold". As discussed above for claim 1 the combination of Yu and Koufopaviou do not teach transferring an exhaustion signal when the number of pointers reach a minimum threshold.

Claim 18 also requires that "in response to the exhaustion signal, creating additional external buffers and their corresponding pointers where the additional external buffers are external to the integrated circuit and are configured to store the communication packets". As discussed above for claim 1 the combination of Yu and Koufopaviou do not teach creating additional buffers in response to the exhaustion signal.

Because there are a number of elements required in claim 18 (discussed above) that are not taught by Koufopaviou et al. in combination with Yu et. al. the examiner has not established a *prima facie* case of obviousness and claim 18 is allowable as written.

Claims 19 – 21, 23 – 28 and 30 – 34 are dependent on allowable claim 18 and are therefore allowable.

Conclusion

In view of the above, applicant respectfully request that the examiner's rejection of claims 6 – 21, 23 – 28 and 30 – 34 be reversed.

The Director is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 502622.

Respectfully submitted,

Date: 8/11/05

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APPENDIX I
CLAIMS CURRENTLY PENDING

1. An integrated circuit that processes communication packets, the integrated circuit comprising:

a core processor configured to create a plurality of external buffers that are external to the integrated circuit and configured to store the communication packets where each external buffers is associated with a pointer that corresponds to the external buffer;

a pointer cache configured to store the pointers that correspond to the external buffers;

control logic configured to allocate the external buffers as the corresponding pointers are read from the pointer cache and de-allocate the external buffers as the corresponding pointers are written back to the pointer cache wherein the control logic is configured to transfer an exhaustion signal if a number of the pointers to the de-allocated buffers reaches a minimum threshold; and

the core processor configured to create additional external buffers and their corresponding pointers in response to the exhaustion signal.

2. The integrated circuit of claim 1 wherein the control logic is configured to track a number of the pointer to the de-allocated external buffers.

3. The integrated circuit of claim 1 wherein the control logic is configured to transfer additional pointers to the pointer cache if a number of the pointers to the de-allocated buffers reaches a minimum threshold.

4. The integrated circuit of claim 1 wherein the control logic is configured to transfer an excess portion of the pointers from the pointer cache if the number of the pointers to the de-allocated buffers reaches a maximum threshold.

5. (Canceled).

6. The integrated circuit of claim 1 wherein the external buffers are distributed among at least

two pools.

7. The integrated circuit of claim 1 wherein the external buffers and the pointers to the external buffers are distributed among a plurality of classes.

8. The integrated circuit of claim 7 wherein the control logic is configured to track a number of the pointers to the de-allocated external buffers for at least one of the classes.

9. The integrated circuit of claim 7 wherein the control logic is configured to track a number of the pointers to the allocated external buffers for at least one of the classes.

10. The integrated circuit of claim 7 wherein the control logic is configured to borrow at least some of the pointers from a first one of the classes for use by a second one of the classes.

11. The integrated circuit of claim 7 wherein the control logic is configured to re-distribute at least some of the pointers from a first one of the classes to a second one of the classes.

12. The integrated circuit of claim 7 wherein the control logic is configured to transfer an exhaustion signal if a number of the pointers to the de-allocated buffers in one of the classes reaches a minimum threshold.

13. The integrated circuit of claim 7 wherein the control logic is configured to track a number of the pointer distributed to one of the classes.

14. The integrated circuit of claim 7 wherein at least one of the classes is associated only with constant bit rate packets.

15. The integrated circuit of claim 7 wherein at least one of the classes is associated only with available bit rate packets.

16. The integrated circuit of claim 7 wherein at least one of the classes is associated only with variable bit rate packets.

17. The integrated circuit of claim 7 wherein at least one of the classes is associated only with unspecified bit rate packets.

18. A method of operating an integrated circuit that processes communication packets, the method comprising:

creating a plurality of external buffers that are external to the integrated circuit and that are configured to store the communication packets,

creating a plurality of pointers where each pointer corresponds to one of the plurality of external buffers;

storing a subset of the plurality of pointers in a pointer cache in the integrated circuit;

allocating the external buffers as the corresponding pointers are read from the pointer cache;

de-allocating the external buffers as the corresponding pointers are written back to the pointer cache;

transferring an exhaustion signal if a number of the pointers to the de-allocated buffers reaches a minimum threshold; and

in response to the exhaustion signal, creating additional external buffers and their corresponding pointers where the additional external buffers are external to the integrated circuit and are configured to store the communication packets.

19. The method of claim 18 further comprising tracking a number of the pointer to the de-allocated external buffers.

20. The method of claim 18 further comprising transferring additional pointers to the pointer cache if a number of the pointers to the de-allocated buffers reaches a minimum threshold.

21. The method of claim 18 further comprising transferring an excess portion of the pointers from the pointer cache if the number of the pointers to the de-allocated buffers reaches a maximum threshold.

22. (Canceled).

23. The method of claim 18 wherein the external buffers are distributed among at least two pools.

24. The method of claim 18 wherein the external buffers and the pointers to the external buffers are distributed among a plurality of classes.

25. The method of claim 24 further comprising tracking a number of the pointers to the de-allocated external buffers for at least one of the classes.

26. The method of claim 24 further comprising tracking a number of the pointers to the allocated external buffers for at least one of the classes.

27. The method of claim 24 further comprising borrowing at least some of the pointers from a first one of the classes for use by a second one of the classes.

28. The method of claim 24 further comprising re-distributing at least some of the pointers from a first one of the classes to a second one of the classes.

29. (Canceled).

30. The method of claim 24 further comprising tracking a number of pointers distributed to one of the classes.

31. The method of claim 24 wherein at least one of the classes is associated only with constant bit rate packets.

32. The method of claim 24 wherein at least one of the classes is associated only with available bit rate packets.

33. The method of claim 24 wherein at least one of the classes is associated only with variable bit rate packets.

34. The method of claim 24 wherein at least one of the classes is associated only with unspecified bit rate packets.